Reliability Report

BE Change Process:

PPAK matrix line in STS with Cu wires

TV1: LDFPT - UA63
TV2 :LDL112PT - UX56

General Information		Locations	
Product Lines	*UA63*	**Wafer fab**	*CTM8+ NiPd PACTECH*
Product Description	Adjustable low drop volt reg (v min 0.8 V - 1A)	**Assembly plant**	*STS*
P/N	*LDFPT*	**Reliability Lab**	*Catania Reliability LAB*
Product Group	AMS		
Product division	General Purpose Analog & RF Power Management		
Package	*PPAK*		
Silicon Process technology	*BCD6S*		

General Information		Locations	
Product Lines	*UX56*	**Wafer fab**	*CTM8*
Product Description	1.2 A low quiescent current LDO with reverse current protection	**Assembly plant**	*STS*
P/N	*LDL112PT*	**Reliability Lab**	*Catania Reliability LAB* *QA Lab SHENZHEN*
Product Group	AMS	**Reliability assessment**	*Pass*
Product division	General Purpose Analog & RF Power Management		
Package	*PPAK*		
Silicon Process technology	*BCD6S*		

DOCUMENT INFORMATION

Version	Date	Pages	Prepared by	Approved by	Comment
1.0	Feb-2018	6	Vito Gisabella	Giovanni Presti	Preliminary Report

Note: This report is a summary of the reliability trials performed in good faith by STMicroelectronics in order to evaluate the potential reliability risks during the product life using a set of defined test methods.
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TABLE OF CONTENTS

1 APPLICABLE AND REFERENCE DOCUMENTS 3
2 GLOSSARY 3
3 RELIABILITY EVALUATION OVERVIEW 3
3.1 OBJECTIVES 3
3.2 TEST VEHICLE 3
3.3 CONCLUSION 3
4 DEVICE CHARACTERISTICS 4
4.1 DEVICE DESCRIPTION 4
4.2 CONSTRUCTION NOTE 4
5 TESTS RESULTS SUMMARY 5
5.1 TEST VEHICLE 5
5.2 TEST PLAN AND RESULTS SUMMARY 5
5.3 TESTS DESCRIPTION 6

1 APPLICABLE AND REFERENCE DOCUMENTS

Document reference	Short description
JESD47	Stress-Test-Driven Qualification of Integrated Circuits

2 GLOSSARY

DUT	Device Under Test
SS	Sample Size

3 RELIABILITY EVALUATION OVERVIEW

3.1 Objectives

To qualify the PPAK matrix line in ST Shenzhen.

3.2 Test vehicle

TV1:LDFPT – UA63
TV2:LDL112PT – UX56

Process changes

TECNOLOGy	LINE PN	CUP	Actual WIRE	New Wire in Matrix	Die Size (mm)	Ground Bonding	COMMENT
BCD6 (+NiPd)	UA63 LDFPT	YES	Au 1.2 mils	Cu 1.0 mils	1.357 x 0.805	8 wires Vout fix / 7 wires Vout adj, Ground wire	
BCD6	UX56 LDL112	NO	Au 1.2 mils	Cu 1.2 mils	0.92 x 0.92	7 wires, No Ground wire	

CUP = Circuit under pads

FE

LDFPT: BCD6 Technology, NiPd PACTECH
LDL112: BCD6 Technology

BE

PPAK in Shenzhen matrix line
Cu wire

3.3 Conclusion

The present report includes the preliminary results on both TVs, UA63 LDFPT and UX56 LDL112.

Qualification Plan requirements will be fulfilled without exception. It is stressed that the available results on reliability tests have shown that the devices behave correctly against environmental tests (no failure). Moreover, the stability of electrical parameters during the accelerated tests demonstrates the ruggedness of the products and safe operation, which is consequently expected during their lifetime.

4 DEVICE CHARACTERISTICS

4.1 Device description

The LDF is a fast, very low drop linear regulator which operates from an input supply voltage in the range of 2.6 V to 16 V. It is available in fixed and adjustable output voltage versions, from 0.8 V to 12 V. The LDF features are: high output precision, very low-dropout voltage, low noise, and low quiescent current, therefore suitable for low voltage microprocessors and memory applications. Current and thermal protection are provided.

The LDL112 is a low-dropout linear regulator, which can provide a maximum current of 1.2 A, with a typical dropout voltage of 300 mV. It is stabilized with a ceramic capacitor on the output. The very low drop voltage, low quiescent current and reverse current protection features make it suitable for low power battery-powered applications. The enable logic control function puts the LDL112 in shutdown mode allowing a total current consumption lower than 1 µA. The device is equipped with current limit and thermal protection.

4.2 Construction note

	LDFPT	*LDL112PT*
Wafer/Die fab. information		
Wafer fab manufacturing location	CTM8	CTM8
Technology	BCD6S + NiPd PACTECH	BCD6S
Die finishing back side	Cr/NiV/Au	Cr/NiV/Au
Die size	1357x805	920x920
Bond pad metallization layers	NiPd	Ti/AlCu/TiNARC
Passivation type	TEOS/SiN/Polyimide	TEOS/SiN/Polyimide
Assembly information		
Assembly site	STS	STS
Package description	PPAK	PPAK
Mold Compound	Epoxy Halogen Free	Epoxy Halogen Free
Die attach	Soft solder	Soft Solder
Bond Wire	Copper 1.0 mils	Copper 1.2 mils

5 TESTS RESULTS SUMMARY

5.1 Test vehicle

Lot #	P/N	Line	Technology	Package	Comments
1st	LDFPT	UA63	BCD6S +NiPd PACTECH	PPAK	Circuit under pads by ST Catania Rel. Lab
2nd					
3rd	LDL112PT	UX56	BCD6S		by ST Catania Rel. Lab
4th					by QA Lab SHENZHEN

5.2 Test plan and results summary

Test	PC	Std ref.	Conditions	SS	Steps	Failure/SS				Note
Die Oriented Tests						1st lot UA63 LDFPT	2nd lot UA63 LDFPT	3rd lot UX56 LDL112PT	4th lot UX56 LDL112PT	
HTOL	N	JESD22 A-108	Ta = 125°C, Bias= Vcc=+2V:+20V		168 h	0/77				
					500 h	run				
					1000 h					
			Ta = 125°C, Bias= Vcc=+7V		168 h			0/77		
					500 h			run		
					1000 h					
HTS	N	JESD22 A-103	Ta = 150°C		168 h	0/25	0/25	0/25	0/80	
					500 h	run	run	run	0/80	
					1000 h				0/80	
Package Oriented Tests										
PC		JESD22 A-113	Drying 24 H @ 125°C Store 168 H @ Ta=85°C Rh=85% Oven Reflow @ Tpeak=260°C 3 times		Final	pass	pass	pass	pass	go no go
AC	Y	JESD22 A-102	Pa=2Atm / Ta=121°C		96h	0/25	0/25	0/25	0/97	
TC	Y	JESD22 A-104	Ta = -65°C to 150°C		100 cy	0/25	0/25	0/25	0/85	
					200 cy	run	run	run	0/85	
					500 cy				0/85	
THB	Y	JESD22 A-101	Ta = 85°C, RH = 85%, 1°Lot Vcc= +2V:+16V		168 h	0/25	0/25			
					500 h	run	run			
					1000 h					
			Ta = 85°C, RH = 85%, 3°Lot Vcc= +5.5V		168 h			0/25		
					500 h			run		
					1000 h					
Other Tests										
ESD	N	JEDEC22- C101	CDM			run		run		
CA			Construction Analysis			run				

5.3 Tests Description

Test name	Description	Purpose
Die Oriented		
HTOL High Temperature Operative Life	The device is stressed in static or dynamic configuration, approaching the operative max. absolute ratings in terms of junction temperature and bias condition.	To determine the effects of bias conditions and temperature on solid state devices over time. It simulates the devices' operating condition in an accelerated way. The typical failure modes are related to, silicon degradation, wire-bonds degradation, oxide faults.
HTSL High Temperature Storage Life	The device is stored in unbiased condition at the max. temperature allowed by the package materials, sometimes higher than the max. operative temperature.	To investigate the failure mechanisms activated by high temperature, typically wire-bonds solder joint ageing, data retention faults, metal stress-voiding.
Package Oriented		
PC Preconditioning	The device is submitted to a typical temperature profile used for surface mounting devices, after controlled moisture absorption.	As stand-alone test: to investigate the moisture sensitivity level. As preconditioning before other reliability tests: to verify that the surface mounting stress does not impact on the subsequent reliability performance. The typical failure modes are "pop corn" effect and delamination.
AC Auto Clave (Pressure Pot)	The device is stored in saturated steam, at fixed and controlled conditions of pressure and temperature.	To investigate corrosion phenomena affecting die or package materials, related to chemical contamination and package hermeticity.
TC Temperature Cycling	The device is submitted to cycled temperature excursions, between a hot and a cold chamber in air atmosphere.	To investigate failure modes related to the thermo-mechanical stress induced by the different thermal expansion of the materials interacting in the die-package system. Typical failure modes are linked to metal displacement, dielectric cracking, molding compound delamination, wire-bonds failure, die-attach layer degradation.
THB Temperature Humidity Bias	The device is biased in static configuration minimizing its internal power dissipation, and stored at controlled conditions of ambient temperature and relative humidity.	To evaluate the package moisture resistance with electrical field applied, both electrolytic and galvanic corrosion are put in evidence.
Other Tests		
ESD Electro Static Discharge	The device is submitted to a high voltage peak on all his pins simulating ESD stress according to different simulation models. **CDM**: Charged Device Model	To classify the device according to his susceptibility to damage or degradation by exposure to electrostatic discharge.
Ca Construction Analysis	Construction Analysis check	To verify the physical product conformity